

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. .... 10/241,245  
Priority Filing Date ..... September 10, 2002  
Inventor ..... Belford T. Coursey  
Assignee ..... Micron Technology, Inc.  
Priority Group Art Unit ..... 2813  
Priority Examiner ..... Yennhu B. Huynh  
Attorney Docket No. .... MI22-2459  
Customer No. .... 021567  
Title ..... Dynamic Random Access Memory Circuitry

**INFORMATION DISCLOSURE STATEMENT**  
**PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98**

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

With the exception of two new references (5,780,338 and 6,114,201 – copies attached), the listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 10/241,245, filed September 10, 2002. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 12-5-03

By:   
Mark S. Matkin, Reg. No. 32,268

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2459		PRIORITY SERIAL NO. 10/241,245	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT: Belford T. Coursey			
				PRIORITY FILING DATE September 10, 2002		PRIORITY GROUP ART UNTI 2813	

  

U.S. PATENT DOCUMENTS							
*Examiner's Initials	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	4,978,009	01/22/91	Flanner				
AB	4,996,627	02/26/91	Zias et al.				
AC	5,023,683	06/11/91	Yamada				
AD	5,032,882	07/16/91	Okumura et al.				
AE	5,061,650	10/29/91	Dennison et al.				
AF	5,084,414	01/28/92	Manley et al.				
AG	5,087,591	02/11/92	Teng				
AH	5,120,679	06/09/92	Boardman et al.				
AI	5,138,412	08/11/92	Hieda et al.				

  

FOREIGN PATENT DOCUMENTS							
Document Number	Date	Country	Class	Subclass	Translation		
					Yes	No	
AJ	2528608	06/14/96	Japan (Micron)				
AK	2-275665	11/09/90	Japan				
AL	3-174765	07/29/91	Japan				

  

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)		
AM		Fujii et al., <i>ULSI DRAM Technology With Ba<sub>0.7</sub>Sr<sub>0.3</sub>TiO<sub>3</sub> Film of 1.3 nm Equivalent SiO<sub>2</sub> Thickness and 10<sup>-9</sup>AJ</i> <i>cm<sup>2</sup> Leakage Current</i> , IEEE 267-270 (1992).
AN		IBM Tech Bulletin, <i>Stacked Capacitor DRAM Cell With Vertical Fins (VF-STC)</i> , 33 IBM TECHNICAL DISCLOSURE Bulletin, No. 2, pp. 245-247 (July 1990).
AO		Kaga et al., <i>Crown-Shaped Stacked-Capacitor Cell for 1.5-V Operation 64-Mb DRAM's</i> , 38 TRANSACTIONS ON ELECTRON DEVICES, No. 2, pp. 255-260 (February 1991).
EXAMINER		DATE CONSIDERED

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS							
*Examiner's Initials	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	5,168,073	12/01/92	Gonzalez et al.				
AB	5,206,183	04/27/93	Dennison				
AC	5,250,457	10/05/93	Dennison				
AD	5,770,499	06/23/98	Kwok et al.				
AE	5,780,338	07/14/98	Jeng et al.				
AF	5,990,021	11/23/99	Prall et al.				
AG	5,998,257	12/07/99	Lane et al.				
AH	6,030,879	02/29/00	Huang				
AI	6,054,394	04/25/00	Wang				

  

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Document Number	Date	Country	Class	Subclass	Translation		
					Yes	No	
AJ	4220497 A1	06/23/92	Germany (Samsung)				
AK	4316503 A1	05/17/93	Germany (Micron)				
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)		
AM		Kawamoto et al., A 1.28 $\mu$ m <sup>2</sup> Bit-Line Shielded Memory Cell Technology for 64Mb DRAMs, IEEE 13-14 (1990
		Symposium on VLSI Technology).
AN		Ueno et al., A Quarter-Micron Planarized Interconnection Technology With Self-Aligned Plug, IEEE 305-308
		(1992).
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U.S. PATENT DOCUMENTS							
*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,057,206	05/02/00	Nguyen et al.			
	AB	6,087,261	07/11/00	Nishikawa et al.			
	AC	6,114,201	09/05/00	Wu			
	AD	6,130,126	10/10/00	Iwakiri			
	AE	6,159,818	12/12/00	Durcan et al.			
	AF	6,200,898	03/13/01	Tu			
	AG	6,232,168	05/15/01	Coursey			
	AH	6,232,240	05/15/01	Tung			
	AI	6,258,729	07/10/01	DeBoer et al.			
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							Yes      No
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	AK						
	AL						
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*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,376,380	04/23/02	Tang et al.			
	AB	6,395,600 B1	05/28/02	Durcan et al.			
	AC	6,426,243 B1	07/30/02	Coursey			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

  

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